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ADVENT

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SATELLITE COMMUNICATIONS PROGRAM

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RESEARCH LABORATORIES
TORRENCE, CALIFORNIA
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(7) [SEQUENCE GENERATOR] (8)

(6) ADVENT COMMUNICATION SYSTEM.

(9) MONTHLY LETTER REPORT NO. 2, ✓

For the Period Covering

26 October, 1960 to 25 November, 1960,

(10) B. Freymodsson R.F. Burman.
Bendix Systems Division Subcontract No. B-1569

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Advent Sequence Generator

MONTHLY LETTER REPORT NO. 2

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1.0 INTRODUCTION

This Monthly Letter Report describes the effort expended and progress made during the period October 26, 1960, to November 25, 1960, in the design and development of the Sequence Generator under Bendix Systems Subcontract No. B-1569.

2.0 PROGRESS

During the period covered by this report, the work effort was directed at the following phases of the program:

- a) Continuation of the Logic Design of the Sequence Generator.
- b) Continuation of the design and development of the 20 MC circuits for the Sequence Generator.
- c) Continuation of the Mechanical Design of the Sequence Generator.
- d) Generation and submission of the following documents related to the reliability effort:
 - 1) "Quality Control and Inspection Plan" Report
 - 2) "Parts and Material Test Plan" Report
- e) Initiation of the construction of a 1 MC Logic Simulator.

Details of the work accomplished in the above phases of the program are further discussed in the subsequent paragraphs.

2.1 LOGIC DESIGN

On October 26 and 27, 1960, a technical BSD-MRL meeting was held at the Torrance facility of the Magnavox Research Laboratories. The minutes of these meetings were formally submitted to BSD in accordance with the requirements of the subcontract as document MRL Control No. 04030.

In Quarterly Report No. 1, (MRL Report No. R-348, MADVT 12-05-01 QR) it was reported that one of the conclusions reached at this meeting embodied modifications of the logic design of the Sequence Generator to a configuration where a 19 stage and a 31 stage shift register would be used instead of the 15-17-19 stage configuration presented in the Design Plan Report. This conclusion was premature for the reasons discussed below.

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Investigation of tabulations of feedback taps for maximal sequences from 19 and 31 stage registers has revealed that approximately 150 distinct maximal sequences (for four-variable feedback) can be generated in a 19 stage register and 8 distinct maximal sequences can be generated in a 31 stage register employing two-variable feedback. This yields approximately 1,000 distinct sequences with periods greater than one year for the 19 and 31 stage configuration. Additional maximal sequences can be generated if six-variable feedback is used in the 19 stage register, or if four-variable feedback is used in the 31 stage register. Tabulation of six-variable feedback for 19 stage maximal sequence is available. On the other hand, search of the literature has failed to yield tabulation of four-variable feedback for maximal sequences from 31 stage registers.

It may be desirable to utilize at least four feedback taps in each register in order to afford greater sequence security. It may further be desired to provide a greater variety of sequences than can be suitably generated with the 19 and 31 stage configuration. In view of these considerations the eventual logic design for the Sequence Generator is not considered finalized as yet.

Currently an effort is being made to secure tabulations of some four-variable feedback connections for maximal sequences from 31 stage registers.

2.2 CIRCUIT DESIGN

Development of the 20 MC circuits for the Sequence Generator has continued during the period covered by this report. Three register stages with a modulo two feedback gate have been breadboarded. Preliminary tests indicate that the 20 MC flip-flop circuit design reported in Quarterly Report No. 1 will afford switching speeds which are commensurate with the operational requirements of the 20 MC Sequence Generator. Substantial circuit refinement will, however, be required before this circuit performs satisfactorily in the plug-in modular configurations that will eventually be used.

2.3 MECHANICAL DESIGN

The major mechanical design effort during this report period has been investigation of approaches to the modularization of the 20 MC circuits. Particular

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emphasis has been placed on surveying the availability of connectors for the plug-in modules with considerations for both reliability and satisfactory circuit performance. Several samples of connectors have been received and are currently being evaluated. Initial effort to package the 20 MC shift register stage on a printed circuit card is in process.

2.4 RELIABILITY EFFORT

In accordance with the requirements of paragraph 3.10 of "Advent Reliability Standards and Quality Control" (BSD No. ADVT 05-03-01 RE), a "Quality Control and Inspection Plan" (MRL Report No. R-351, MADVT 12-07-01 TP) was generated and submitted to BSD on November 15, 1960. This document details the procedures and establishes responsibilities for the quality control effort in support of the Sequence Generator program.

In accordance with the requirements of paragraph 3.8.1:1 of "Advent Reliability Standards and Quality Exhibit" (BSD No. ADVT 05-03-01 RE), a "Parts and Material Test Plan and Procedures" (MRL Report No. R-352, MADVT 12-08-01 RR) was generated and submitted to BSD on November 15, 1960. This document establishes the procedures and details responsibilities for implementing tests of parts and materials for the Sequence Generator.

In accordance with the requirements of paragraph 4.21 of the Statement of Work, a "Preliminary Parts and Material List" was generated. This document will be submitted to BSD by November 30, 1960.

Since the circuit design has not been frozen yet, it is anticipated that changes in this parts list will occur before the circuit design is frozen on February 15, 1960. It is, however, anticipated that such changes will not affect the basic component types that are tabulated in the Preliminary Parts and Material List.

A pre-design environmental study has been conducted in accordance with the requirements of "Advent Reliability Standards and Quality Exhibit" (BSD No. ADVT 05-03-01 RE).

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The results of this study indicate that all the environmental requirements set forth in paragraph 3.5 of "Exhibit, Sequence Generator, Part of the ADVENT Communication System" (BSD Exhibit No. 2323000, 1 September 1960) can be met.

It is anticipated, however, that it will be difficult to meet the 2000 hour MTBF specified in paragraph 3.4.1 of the Exhibit, Sequence Generator. Since the component part failure rates which shall be used in reliability computation for the Sequence Generator have not been established yet, the severity of this problem is not known precisely.

In order to enhance the attainment of the 2000 hour MTBF reliability characteristics, it is proposed that paragraph 3.5.2.2 of BSD 2323000 be modified as follows:

"3.5.2.2 Temperature

3.5.2.2.1 Normal operation - ambient temperature from 40 degrees F to 100 degrees F.

3.5.2.2.2 Emergency operation - ambient temperature from 0 degrees F to 130 degrees F."

The above proposed modification assumes that the Sequence Generator will be used in a computer environment. The temperature range for Emergency Operation is based on the assumption that heating or air conditioning equipment which might normally be used has failed.

The degree of improvement in reliability that can be realized by this reduction in the temperature range for normal operation cannot be determined precisely at this time because the basic component failure rates to be used have not been established. It is pointed out that these component failure rates shall be coordinated through the Bendix Systems Division in accordance with paragraph 3.7 of "Advent Reliability Standards and Quality Exhibit" (ADVT 05-03-01 RE). It is accordingly requested that Bendix make this information available to Magnavox at the earliest possible date.

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2.5 LOW FREQUENCY LOGIC SIMULATOR

During this report period, construction of a low frequency (approximately 1 MC) logic simulator was initiated. This simulator will be used to study the characteristics of the sequences that will be generated by the selected logic design. This low frequency logic simulator will have sufficient flexibility to simulate a large variety of logic configurations for combination of registers with a total of up to 52 stages. The low frequency simulator will be used to study sequence characteristics in both the frequency and time domains and in particular both auto and cross correlation properties.

3.0 PROGRAM STATUS

Following is a brief description of the status of the program milestones specified in Bendix Systems Division Schedule T-302-10.

<u>Milestone</u>	<u>Percentage Completion</u>
Design Plan Report	100% and submitted
Preliminary Logic Design Review	100%
Test Plans and Procedures Parts	100% and submitted
Preliminary Parts List	100%, submitted 29 November 1960

4.0 FUTURE PLANS

The following activity is planned for the report period covering 26 November, 1960, to 25 December, 1960.

- a) Refinement of the Logic Design for the Sequence Generator will be continued.
- b) Circuit development and mechanical packaging effort will be continued.
- c) Construction of Low Frequency Logic Simulator will be completed.
- d) A technical conference with BSD and MRL personnel participation will be held at the Torrance facility of MRL for the purpose of discussing the technical aspects of the MRL effort and to discuss and resolve interface problems.

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